

Mixed Signal Systems, Inc.



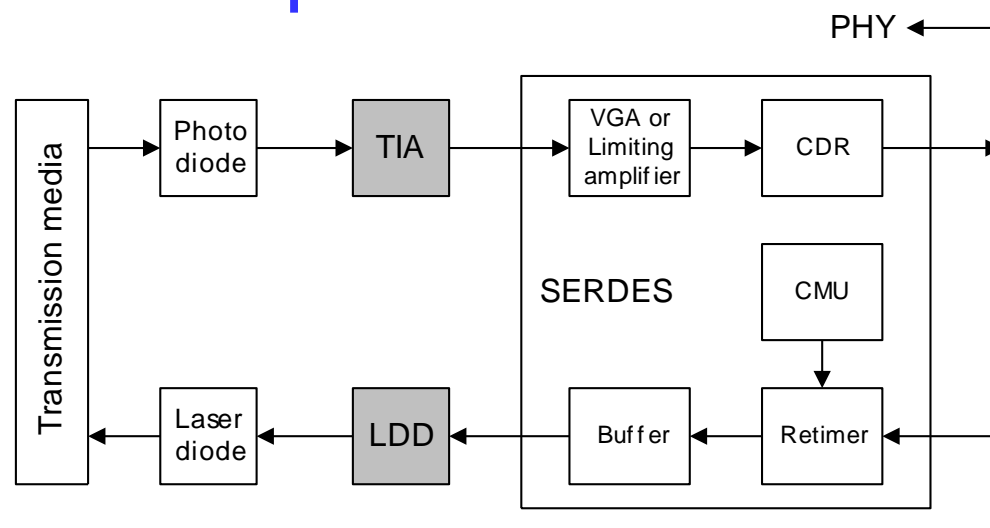
Introduction

- The information contained in this presentation contains examples of the type of designs that Mixed Signal Systems has been responsible for in the past. The intention is to show some of the target markets and the type of circuits blocks that can be realistically integrated.
- In general the performance requirements of the circuits will depend on the application and the circuit performance will depend on the design skills and chosen process.
- Usually there are many trade off factors speed/power/price/complexity/timeframe.
- Good partnerships are essential to successful project completion.

Design and Product background overview

- PLL's from 30 MHz to 16 GHz.
- SERDES circuits from 2.5 Gbps to 10 Gbps.
- RF radio blocks from 900 MHz to 9 GHz.
 - LNA, Mixers, Up/Down converters, Filters, PA's, AGC, ADC.
- UWB: OFDM and DSS – main focus PLL's.
- Extensive on chip VCO experience: LC, Rings.
- 10 Gbps optical communications including TIA, LDD and Limiting Amps.
- High speed (4GHz) low noise dividers for frequency synthesizer applications.
- Read/Write Channels for mass storage up to 350Mbps.

Optical PHY components



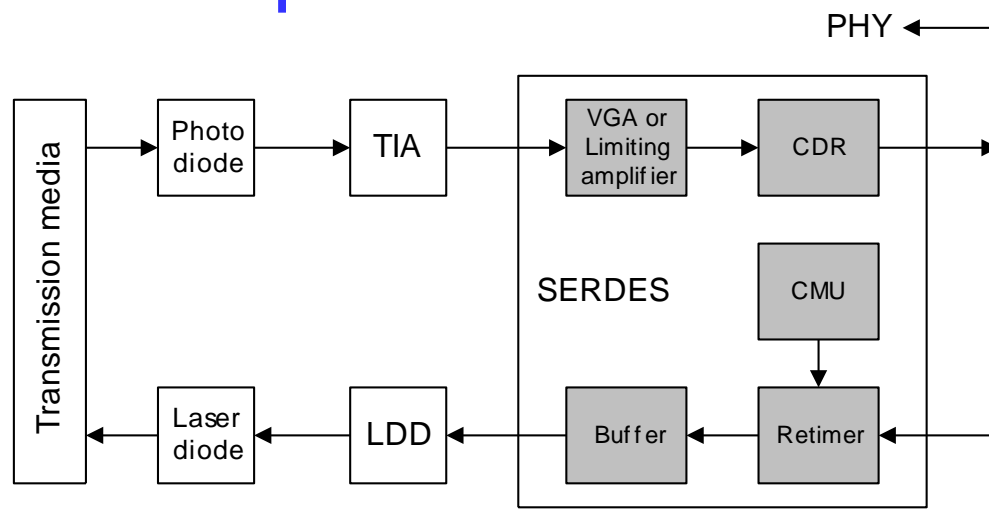
Trans-impedance amplifiers (TIA)

- For these standards:
 - OC-48, OC-192 & GPON
 - 622Mbps, 2.5Gbps, 10Gbps & 1.25Gbps
- Processes: Bipolar, BiCMOS, CMOS
- Invented simple gain compression technique to extend input dynamic range (US patent 6583671)
- Integrated DC compensation loops
- Single and multi channel versions

Laser Diode Driver (LDD)

- For these standards:
 - OC-48, OC-192
 - 1.2Gbps, 2.5Gbps, 10Gbps
- Processes: Bipolar, BiCMOS
- Adjustable bias and modulation current
- Auto shutdown
- Auto power control
- Programmable extinction ratio control
- LDD power monitor
- Duty cycle compensation

Optical PHY components



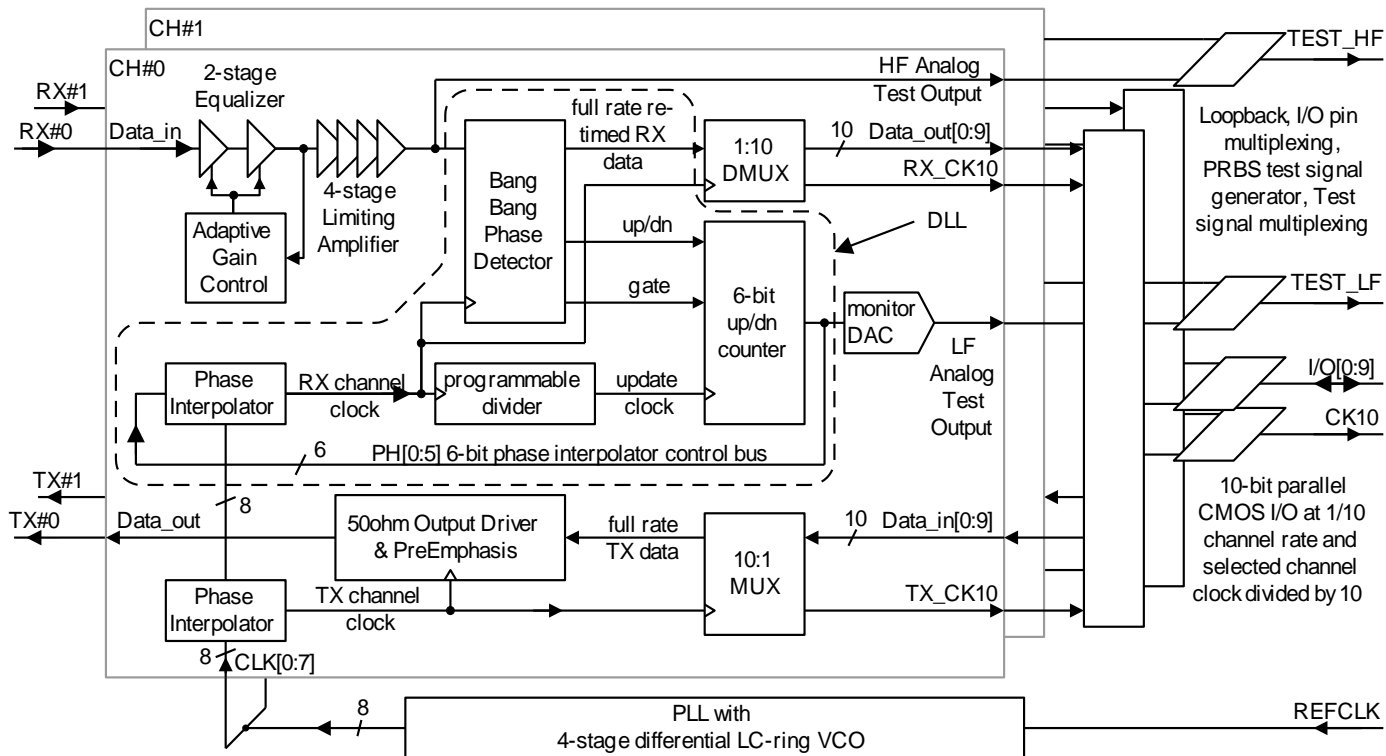
SERDES (1)

- Includes:
 - variable gain amplifier, clock and data recovery unit, clock multiplier unit, 10Gbps 50ohm output
- Presented at ISSCC 2007, "A 250mW Full-Rate 10Gb/s Transceiver Core in 90nm CMOS Using a Tri-State Binary PD with 100ps Gated Digital Output".
- Input sensitivity 5.9mVpp for $1:10^{-12}$ BER
- Jitter tolerance >0.505 UI at 80MHz
- TX jitter generation 5mUI rms, RX clock jitter 910fs rms
- TX rise/fall time 27ps

Wireline PHY components

SERDES (2)

- 3Gbps dual channel transceiver
- Equalizer for extended range across 72" of FR4
- Power <120mW/channel
- Receiver is entirely digital
- RX Jitter tolerance 0.4UIpp @ 80MHz and BER=1:10⁻¹²
- TX jitter generation = 2.6ps rms



Wireline PHY components

Multi-rate Data Transmitter

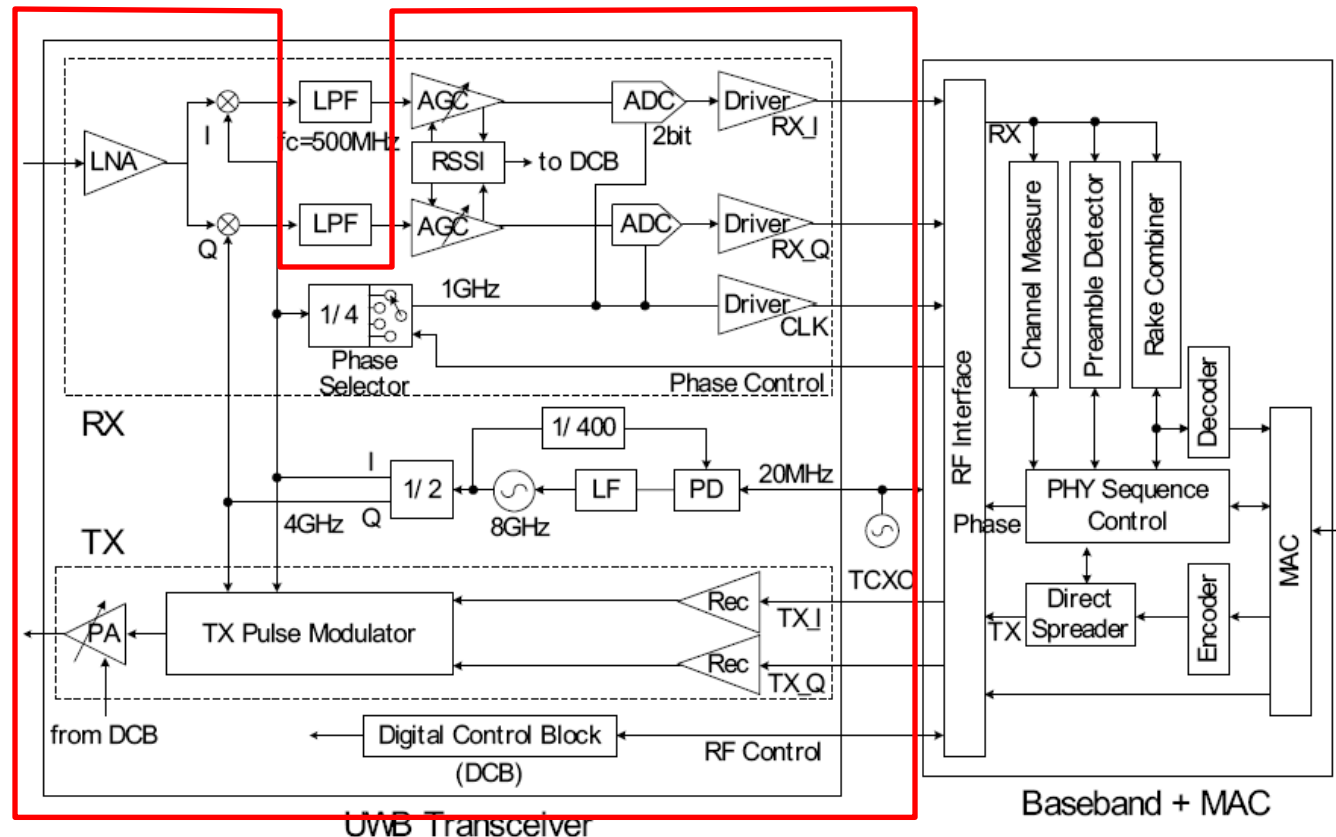
- Synthesizers to cover variable data-rates over a 15:1 continuous frequency range up to 2.5Gbps
- 90nm plain CMOS process (no inductors)

Multi-rate Data Receiver

- Companion to multi-rate transmitter
- 90nm clock and data recovery unit

Wireless PHY components

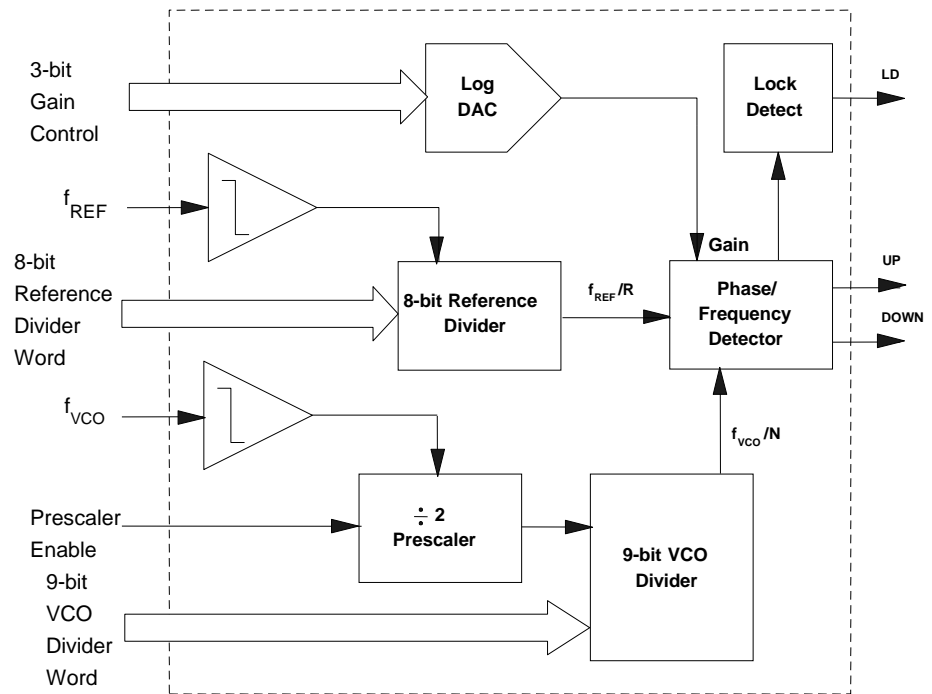
Presented at ISSCC 2005, "A 3.1 to 5GHz CMOS DSSS UWB transceiver for WPANs".



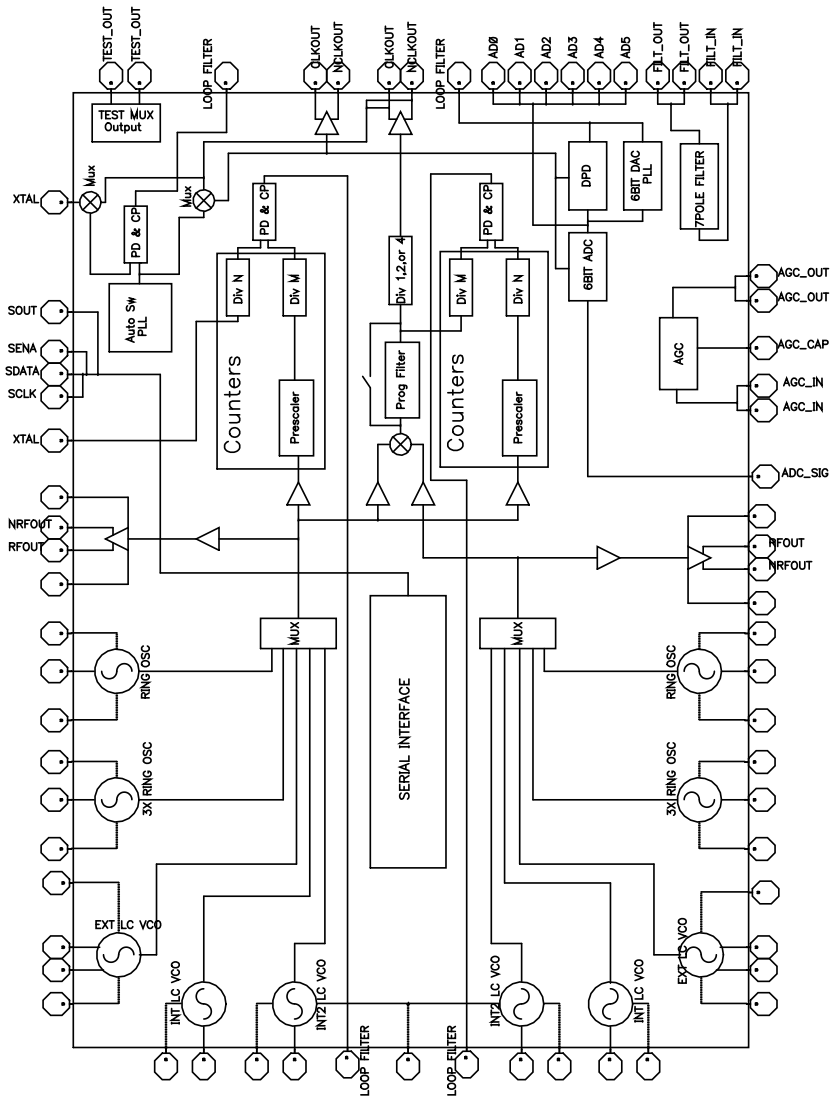
PLL	VCO frequency	8GHz
	LO Phase noise	-125dBc/Hz @ 10MHz
	Lock up time	< 10ms

High speed Dividers

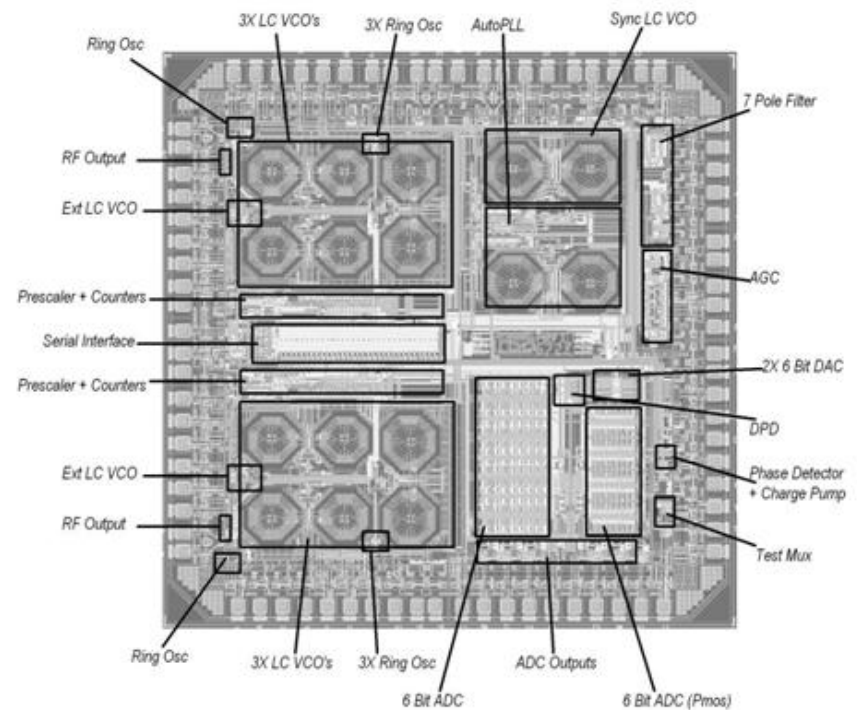
- Input Power range:
 - -10dBm to + 10dBm referenced to 50Ω
- Phase Noise <-160 dBc/Hz at offsets >5kHz
- 4GHz Input Frequency (With Pre-scalar)
- 250MHz Phase/Frequency Detector with Lock Detect
- Analog/Digital Gain Control



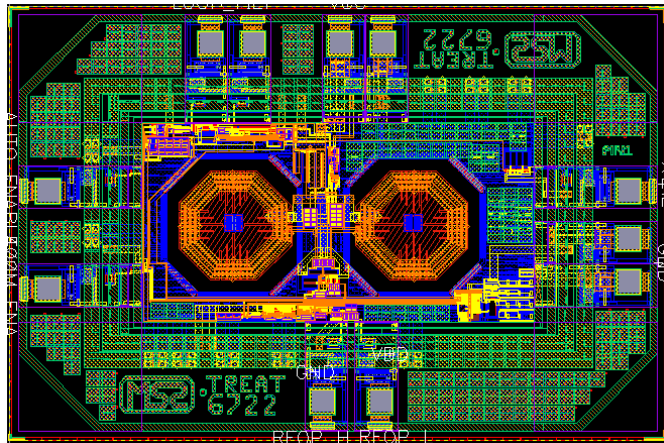
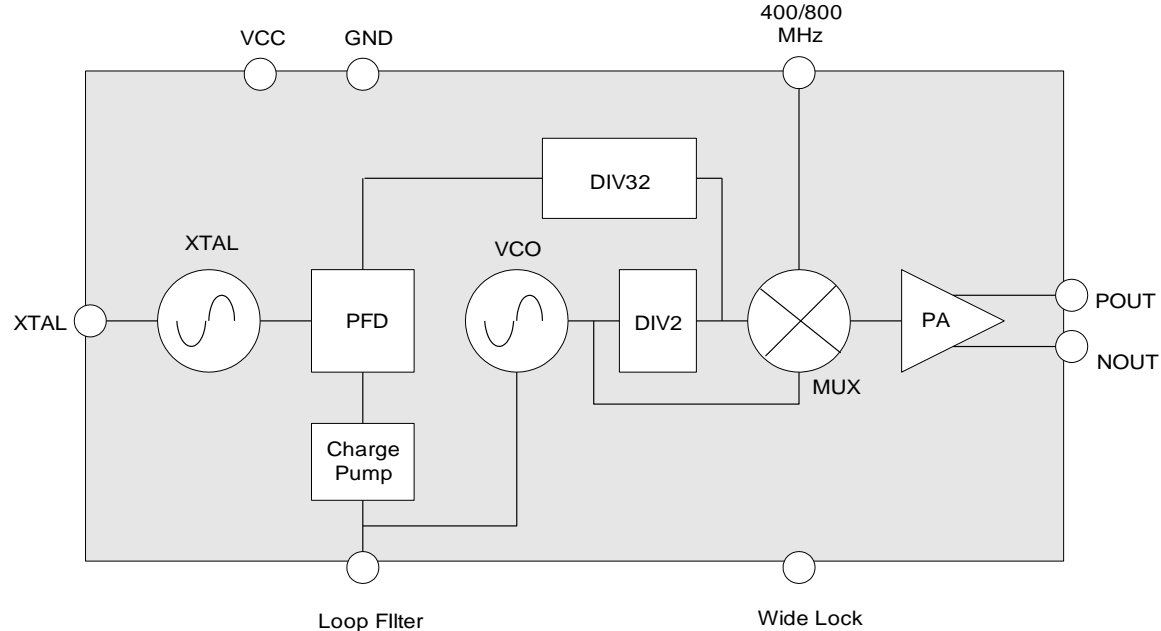
Generic RF chip MS26721



- Fully integrated, highly programmable RF integrated circuit.
- 4GHz max frequency, 0.35um CMOS
- Comprising of 14 selectable High Frequency VCOs, Prescalers, Synthesizers, ADCs, DACs, PLL's, AGC, 7Pole Filter



RF chip MS26722



- Fully integrated PLL with a selectable 400/800 MHz RF output on 0.35um CMOS
- Wide tuning range, 370MHz to 430MHz and 740MHz to 860MHz.
- The RF output is a differential open drain output.
- Low supply (3V) and a low standby current (<1uA)
- Well suited for portable applications.

Mass Storage Devices

- R/W HDD preamps
 - thin film and MR heads
- Read channels - HDD
 - For peak detect and PRML analog front ends
 - US Patent 6307693 - Integration of filter into read/write preamplifier integrated circuit
- Read Channels – optical drives
 - Analog front end
 - Servo PLL control, Data recovery
- Read Channels – Tape
 - Analog front end