Mixed Signal Systems, Inc. – Quick Fact Sheet – Jan 2016

Fabless Integrated Circuit Design and IP Generation

Incorporated August 1991

Key Areas of Expertise:

- PLL components:
  VCO, DIV, CP & PD, PFD
- PLL systems:
  low jitter clock generators
  - timing recovery for read channels
  - SERDES
  - synthesizers for radios
- Optical/Electrical Interface
  - Transimpedance Amp
  - VCSEL/Laser Diode Driver
  - Limiting Amp / AGC
- RF components and systems:
  - mixers, LNA, PA
  - narrowband and UWB
- Process Experience:
  - CMOS down to 28nm
  - Bipolar/BiCMOS/SiGe
- Frequencies – 12Gbps and beyond
  Low power design
  Very low phase noise VCO
  High level system design & modeling

Selected co-authored Publications, co-developed with partners

- IEEJ 2000, International Analog VLSI Workshop:
  "The design of a 3GHz Voltage Controlled Oscillator with On Chip Resonant Tuning Network and Active Frequency Doubler "
- ISSCC 2003:
  "Low-noise monolithic oscillator with an integrated three-dimensional inductor"
- ISSCC 2005:
  "A 3.1 to 5 GHz CMOS DSSS UWB transceiver for WPANs"
- ISSCC 2007:
  "A 250mW Full-Rate 10Gb/s Transceiver Core in 90nm CMOS Using a Tri-State Binary PD with 100ps Gated Digital Output"
- ISSCC 2016: Session 10.4
  "A 12Gb/s 0.9mW/Gb/s Wide-Bandwidth Injection-Type CDR in 28nm CMOS with Reference-Free Frequency Capture"

Patents

- 16 patents – MS2 inventors
  - 8 patents related to PLL implementation
  - 4 patents related to Optical/Electrical interface implementation
  - 4 patents related to RF and analog signal processing
- 1 patent – related to RF – MS2 + Partner co-inventors

What we can do

- Develop IP – at circuit level and system level
- Develop lower power solutions
- Migrate IP across technology generations

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